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THIN FILM TRANSISTOR ADDRESSED DISPLAY DEVICE.(U)
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Research and Development Technical Report

Report ECOM- 72-0061-11

AD A044077

THIN FILM TRANSISTOR-ADDRESSED DISPLAY DEVICE

T. P. Brody
F. C. Luo
D. H. Davies
E. W. Greeneich

WESTINGHOUSE ELECTRIC CORPORATION
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August, 1977

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Eleventh Quarterly Report for Period - September 1976 - December 1976

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T. P. Brody, F. C. Luo, D. H. Davies,
E. W. Greeneich

August, 1977

Contract No. DAAB07-72-C-0061

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Westinghouse R&D Center
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This is the eleventh quarterly report on Contract DAAB07-72-0061. During this period we have improved the quality level of the 6" x 6" 30 lpi TFT-EL displays. In addition we have rebuilt the jigs and tooling and fabricated 30 lpi displays using a new format. This format was designed to be compatible with the ECOM-ARTADS Digital Message Device. A few runs with the new tooling resulted in reasonably good quality displays in the new format.		

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1. Introduction

Up to this reporting period we have demonstrated the following:

- Excellent, near defect free, thin film transistor addressed electro-luminescent (TFT-EL) displays at 20 lines per inch, 6" x 6".
- Reasonable quality TFT-EL displays at 30 lines per inch, 6" x 6".
- A process to increase the elemental lit area per cell to >70%.
- The achievement of drift-free stable high voltage, low leakage TFTs.

In this report we will discuss the continuation of the 6" x 6", 30 lines per inch work; the achieving of good quality (low defect count) displays that utilize a reliable second-level output electroding process is detailed. In addition we report on the modification of the technique that alters the format to a design that allows direct compatibility with an existing Army TACFIRE system component, the ARTADS-Magnavox Digital Message Device (DMD). A convincing demonstration of the wide format universality of the concepts was achieved; within a very few fabrication runs reasonable quality DMD configured displays were made

Further, the design of the elemental cell thin film layout in this DMD configured display was made compatible with alternate production-type processes. This indicates that all other factors being equal it should be possible to fabricate such displays with methods more amenable to mass-production methods. Finally the results of a continuing TFT test program are given. The test now has accumulated over 20,000 hrs.

of continuous operation with only a minor change in TFT threshold that has no significant impact on display operation. Projections from the data indicate that we could expect >200,000 hrs. of operation (25 yrs) and still be well within the allowable transistor threshold operational range.

2. Improved Deposition Methods for Enhanced Thin Film Circuit Fabrication

Major improvements were previously achieved in the display defect count through improved substrate and mask cleanliness. Further refinements in these processes failed to significantly further improve the defect level. Yet detailed tracing of individual defects (elements on or off uncontrolled by the bias levels, shorted busbar crossovers and "opens" in the thin film circuits) indicated that particulate contaminants were still evident in the films at each defect spot. Analysis has indicated that a partial cause of these is "in-system" particulates, i.e. metal flakes generated in the vacuum system itself due to films peeling off the walls and jig surfaces. The particulates settle and are not significant during operation but are swirled through the chamber during roughing, (the initial chamber evacuation by the rotary pump). To eliminate these we have adopted a procedure whereby the mask X-Y set is closed and the substrate clamped to it during this roughing procedure. This seals the mask and substrate surfaces and prevents particulate pick up. Although this procedure has helped it was found not to be a complete answer. The film quality still needed improvement, black irregular inclusions still existed in both metal and

dielectric films. Fig (1) illustrates some of these microscopic defects. The species shown, although small, are still sufficient to cause shorting in the component. After much experimentation we have now achieved a significant reduction in this problem through more effective degassing of the source materials, more uniform sweep on the e-beam gun and the use of a modified e-beam gun; the AIRCO ST1H-2A. The new gun incorporates a rotating hearth surround rather than a static one and this has helped. Fig (2) illustrates a typical 6" x 6" 30 lpi display in operation. The quality level has improved since the last period although further advances are required. We have examined and traced individual defects in these latest displays. On first examination the bulk of the defect causing particulates, such as shown in Fig (1), have been removed. However we have examined such circuits in a high power dark field microscope. Under these conditions it is clear that we still have a particulate defect problem but now we are dealing with a small class of particles. Fig (3) illustrates these sub-micron level defect species in dark field microscopy.

3. Development of a Reliable Second-Level Electroding Process

We use a laminar resist as an insulation layer and to provide isolation between a top electrode and the thin film transistor circuits. This multi-layer approach was perfected in previous months, however, test operation indicated that some first to second level contacts were not reliable. The failure mode leaves the original output pad still lit thereby indicating the elemental circuit is still functional but

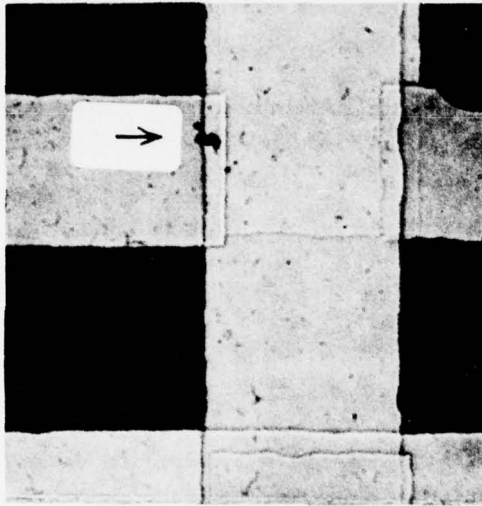


Fig. 1. Microscopic Defect Site in Thin Film Circuit



Fig. 2. Improved Level of Operation in 6" x 6", 30 lpi
2 Level Electroded TFT-EL Display

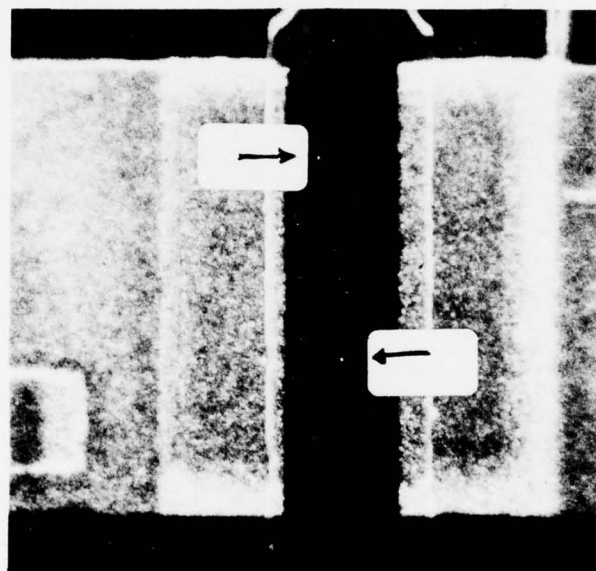


Fig. 3. Dark Field Photomicrograph of Residual
Defect Causing Species

that the contact to the top pad has opened, see Fig (4). Detailed examination revealed that the photoresist was lifting and breaking the contact. After several attempts a process that post-hardens the resist at the contact interface with the glass was developed. Reverse exposure with long wavelength ultraviolet is used; the EL output contact pad of the TFT elemental circuits being used as the self-aligning "photomask."

This process appears to work very well, since incorporation we have not seen evidence of first to second level failure.

4. Translation of Process to Alternate Format

As a result of a contract modification the process was now adapted to change the format of the display from 6" x 6" to 3.4" x 7.0" (2.9" x 6.6" active). This latter format is compatible with the Magnavox Corporation's-ARTADS Digital Message Device (DMD). It was decided that no basic elemental circuit changes were needed and the same thin film material system would be used. The display is 8 x 32 characters (256) or 77 x 222 lines when fully populated. The elemental resolution is there ~ 30 lpi, close to what was being fabricated at 6" x 6".

It was determined that the following actions were required to implement this change.

- (1) Jig modifications needed
 - (a) Notch out interior plates for new area
 - (b) New substrate holder for new format



Fig. 4. Second Level Output Pad; Contact Failure

- (c) New mask holder
- (d) New magnet holder
- (2) New X-Y masks for circuit fabrication needed. It was decided that these would be exactly to the required format but should have extra lines for flexibility and be on the required 750 μm /950 μm basis.
- (3) New edge connector masks needed. Must pick up alternate contacts to pull out source and ground in appropriate direction.
- (4) Riston process. It was decided to generate a new photoplate via metal master and contact print as needed.
- (5) New glass substrates needed. They can be provided by Corning Glass.

All these tasks have been achieved and the new jig is in use. No significant problems were met except for the edge contact. The picking out of the contacts with each separate block in different directions was difficult. Several new methods are being tried. Meanwhile initial displays were made with "single edge" source and gate contacts.

The overall design for the new display is shown in Fig (5). The elemental resolutions are 750 μm in the horizontal and 950 μm in the vertical. The active display area is 2.9" x 6.6" and the display has 225 x 80 lines, all 17,920 elements are addressable. A ~ 0.25 " edge contact border surrounds the active area.

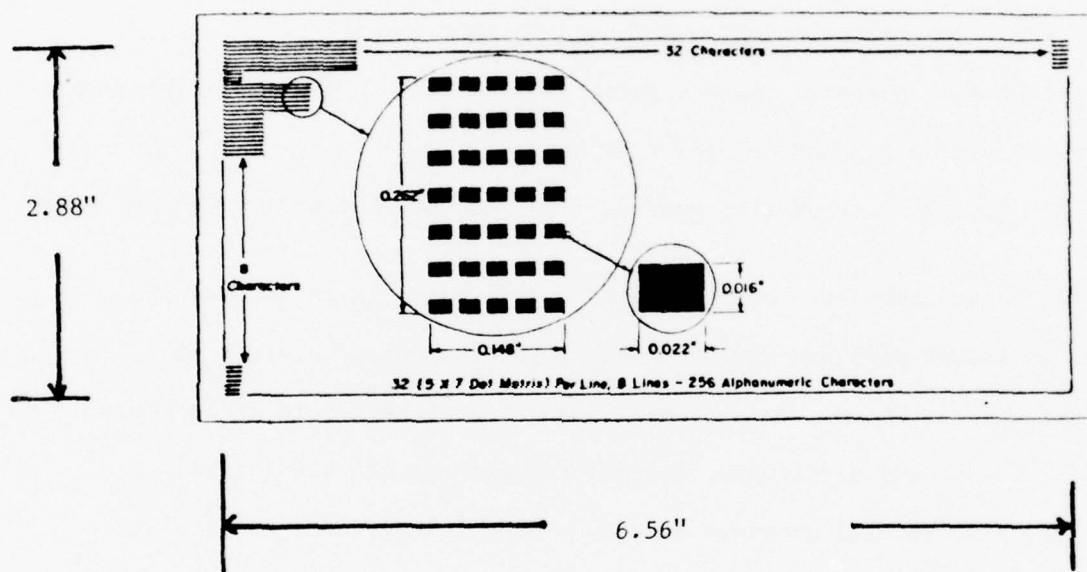


Fig. 5. Format of New Display

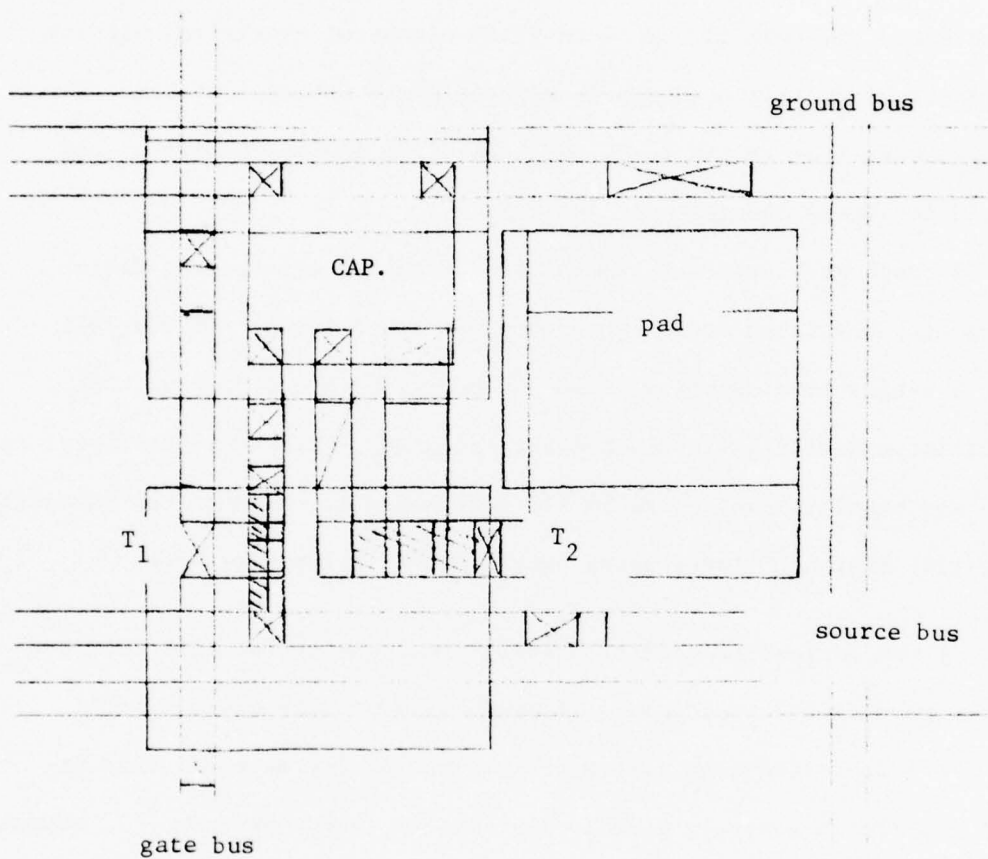


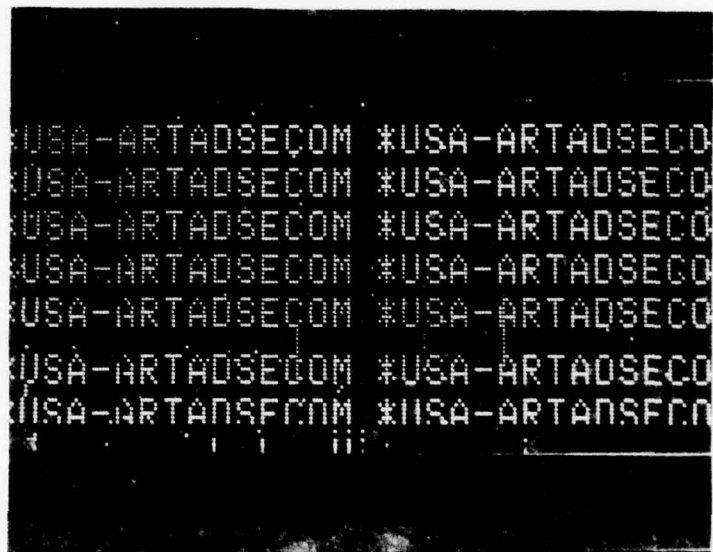
Fig. 6. New Cell Layout Used in X-Y Display Fabrication

5. Results Achieved with New Format

After very few runs displays were made with reasonable performance levels; although not perfect the displays are a convincing demonstration of the ease of translation to a new format. Fig. (7) illustrates the results. Note that the elemental electrical circuit is identical to that used previously as is the material system. Some changes were made in the individual thin film layouts however. The reason for these changes were two-fold.

(a) Through more detailed examination of layout tolerances, design rules etc. developed over several years of experience. it was felt that a single-level display could be made with this format without significant sacrifice in the percent lit area. This is both simpler to make and possibly could have better life since it excludes the potentially sensitive Riston^(R) layer being overlaid with a top electrode.

(b) It was decided to utilize a layout that was appropriate from a future "production" standpoint. A production process would most likely require a dedicated mask system rather than an X-Y method. This in turn requires a computer aided design system (e.g. Applicon^(R)), computer controlled photoplate pattern generators and complex patterned masks. These constraints result in a complex set of design rules that limit layout designs. In association with Contract DAAB07-76-C-0027 a detailed design base following those rules has been obtained and the X-Y layout used in this program was based on those rules. Fig (8) shows the optimum layout as actually fabricated. As can be seen from Fig (7) successful displays have been made in this format; further improvements are expected as more attempts are made at this format.



A black rectangular box containing a grid of text in DMD format. The text is arranged in two columns, with each line consisting of two identical strings separated by a space. The strings are: *USA-ARTADSECOM, *USA-ARTADSECO, *USA-ARTADSECO, *USA-ARTADSECO, *USA-ARTADSECO, *USA-ARTADSECO, and *USA-ARTANSFCOM. The text is white on a black background.

*USA-ARTADSECOM	*USA-ARTADSECOM
*USA-ARTADSECOM	*USA-ARTADSECO
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*USA-ARTADSECOM	*USA-ARTADSECO
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Fig. 7. Operational Performance Level Achieved in DMD Format

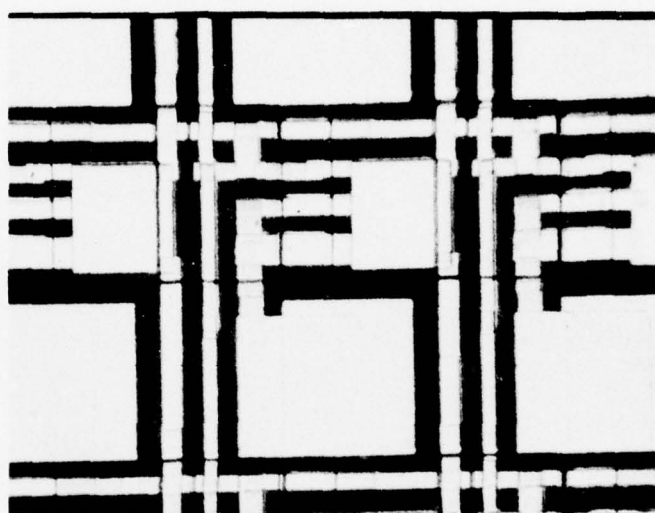


Fig. 8. New Elemental Cell Layout As Actually Fabricated

6. Considerations Regarding Display Life

The factors raised by life requirements can be divided into three principal areas.

1. Brightness deterioration that will occur with operation.
2. Defects that could occur, elements or lines turning on or off and not being controllable. These could arise because of shorts or opens in the circuit.
3. Changes in the TFT properties with operation that could cause the elements to drift out of specification. This applies to the circuit plate somewhat but is more significant if we wish to pursue integrated peripheral scanning circuits.

We are confident that we can satisfy these conditions for the following reasons.

The change in EL brightness with operating life is known and definable under comparable drive and process conditions to those required here. Half lives of >5000 hr have been observed with this fabrication method, the phosphor following the slow decay relationship shown in Fig.(9). This figure is a revision of prior data⁺ where a somewhat longer half life was indicated. Recent results have shown that life is strongly dependent on the method of forming the EL layer. Using a brush type approach to phosphor deposition results in a higher phosphor/binder ratio. The result is that the embedded phosphor layer has somewhat longer life than if a high binder content is present.

⁺Quarterly Report #4.

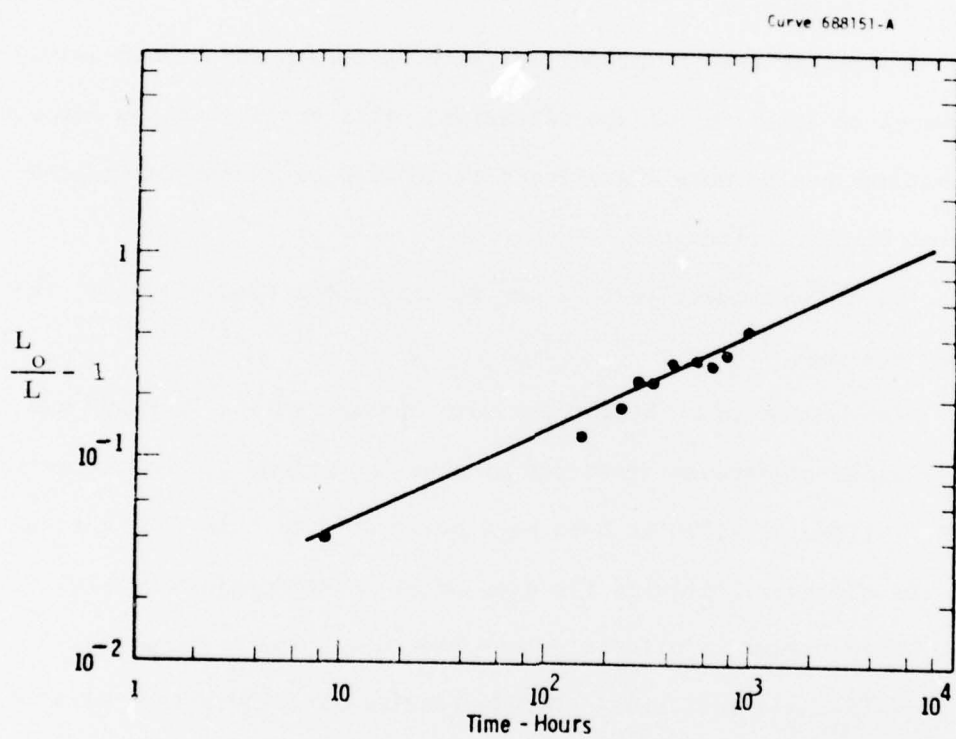


Fig. 9. Phosphor Life Relationship

The method now used to fabricate displays (spray) results in a higher binder ratio in the eventual layer. We have discovered, therefore, that a more realistic figure for a half-life for phosphor layers prepared in the same fashion as the display is $\sim 6,000$ hr (see Fig. (9)). Two factors alleviate this condition somewhat:

1. We are attempting to review our phosphor layer deposition method to incorporate the better methods used in the earlier life tests. This includes silk screening of the phosphor rather than spraying it and also includes the incorporation of a thin (800 \AA) dielectric film over the phosphor. The latter prevents lateral leakage and can be used to enhance contrast.

2. It is possible to still meet, with adequate leeway, good operational life times. Using the relationship of Fig (9) and the phosphor voltage/brightness relationship, it is possible to convert a 1000 hr requirement (say) into drive voltage. We have determined that 40 fL is more than sufficient to meet 2000 fc legibility. To be able to achieve this after say 1000 hr requires that the matrix circuit be capable of handling a drive voltage equivalent to L_1 , where L_1 is derived from the value of $(L_1/L_0 - 1)$. When $t = 1000$ hr in Fig (9) this is ~ 0.40 . Therefore $L_1/L_0 = 1.40$ and since $L_0 = 40$ fL, then $L_1 = 56$ fL and the required voltage drive condition is $\sim 90 V_{\text{rms}}$. This is only marginally above the initial drive requirement of $80 V_{\text{rms}}$ and is well within the capability of the matrix and TFTs. This surprisingly small increase in the maximum voltage rating comes about because of the superlinear brightness/voltage relationship inherent in EL phosphor.

The question of TFT matrix "life" is well documented and reference is made^{1,2} to previous publications on this topic. Two major factors are important: the appearance of defects (related to matrix shorting) and device drift. Two classes of defects are present in the display -- initial defects and those that appear during life. The former are counted as scrap and are not, therefore, under consideration. The latter we have found come under two categories: those which appear in the first few hours of operation due to poor quality crossovers or devices and those which appear during regular operation. Our experience is that the vast majority of defects appear during the first few hours of life. After this it is relatively rare to observe a defect appearing if the voltage used in the initial burn-in is not exceeded. This phenomenon, called "infant mortality," is common to all integrated circuitry. Based on this, we conduct a 2-hr burn-in at the maximum voltage rating after each display is fabricated. A failure here is considered part of fabrication yield, not life. (The question of initial "as fabricated" defects is discussed in Section (2) above).

Transistor threshold drift is a phenomenon that does occur, as indeed it occurs with all silicon MOSFET transistors. With regard to the matrix transistors, it is of relatively little significance, as has been discussed previously. The effect of drift on alphanumeric or other non-gray level displays is minimal since the devices are operating in a saturation mode. However, this is not the case for the peripheral scanning circuits. To test stability, in a mode not significantly different from the operation of the scanning circuits, the following test was conducted.

The test circuit for this study was a free-running astable multivibrator that was discussed in detail in the Ninth Quarterly Report.

Prior to the start of the test, curve tracer I-V characteristics were obtained on device T_1 . The circuit was then started and left to run continuously. The LED flashes at roughly a 1 Hz rate, and periodic data was obtained simply by measuring (with a stopwatch) the time required to generate 100 pulses. The data are shown in Fig (10). After 20,000 hr of operation, I-V characteristics were again taken on T_1 , which were very nearly identical to the original set except for a slight shrinking due to a small shift in threshold voltage (approximately 0.3V) as a result of slow electronic trapping. There is no evidence of fast trapping as indicated by the equivalent of pulsed-mode characteristics and dc characteristics.

The change in the pulse period after 20,000 hr of continuous operation was 15% and can be attributed to the shift in V_T . This change in V_T with time is essentially logarithmic, so we would expect another 15% shift after 200,000 hr (25 years). The I-V characteristics before and after the test are shown in Fig. (11).

These minor changes in V_T are not significant in the operation of the display or indeed the scanning circuit. It is clear, therefore, that the technology can satisfy, say, a 1000 hr life requirement. To be sure, we cannot at this stage point to extensive life data on existing displays. Such experiments are being set up now as part of the present MM&TE program.⁺ Initial data on 6 x 6 in. displays indicates

⁺USA ECOM Contract DAAB06-76-C-0027

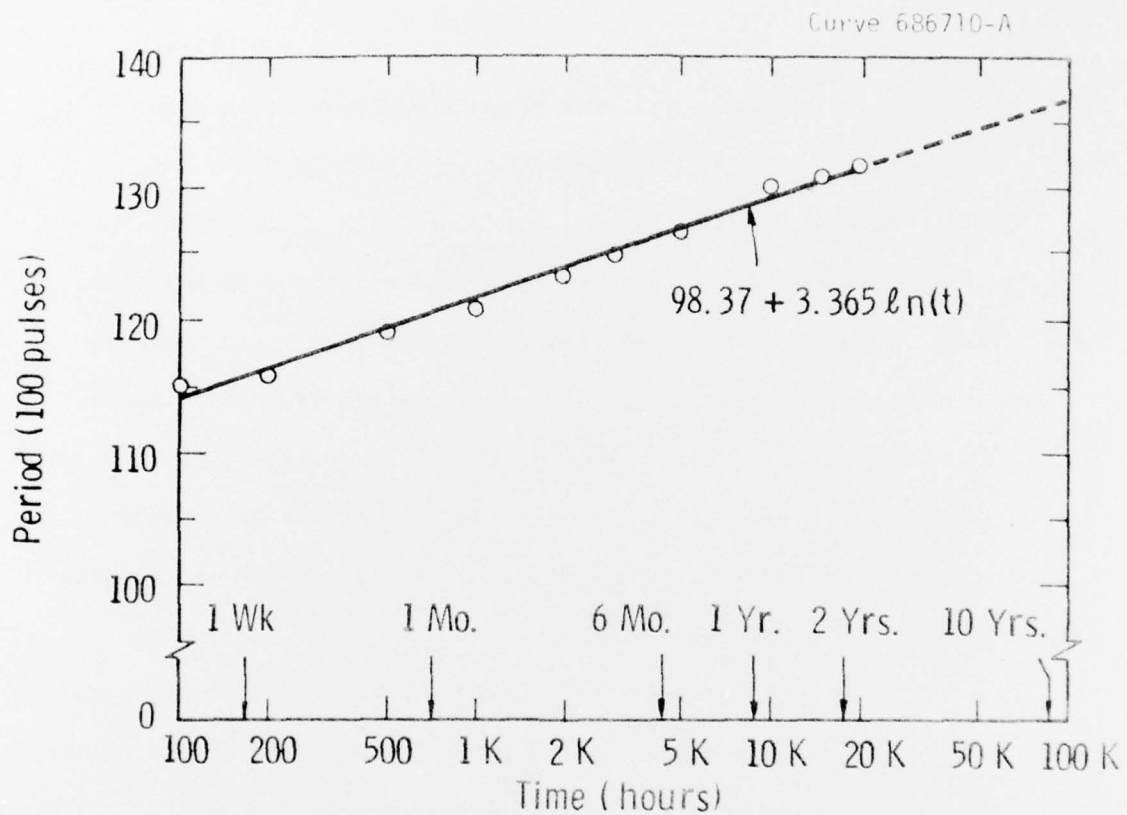
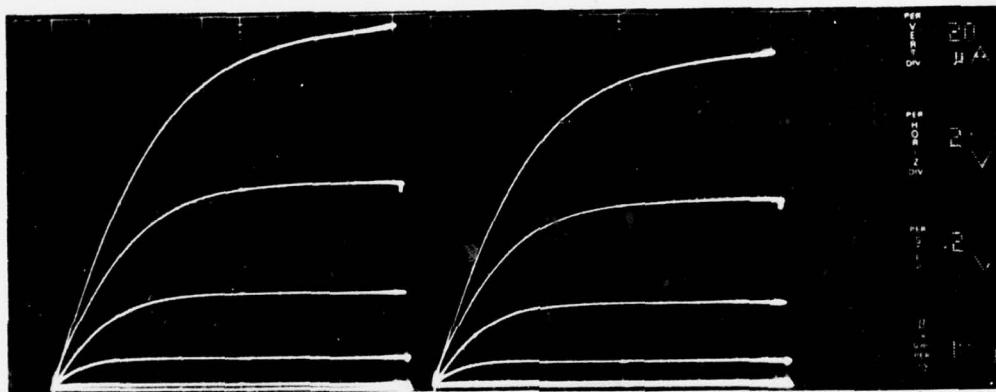


Fig. 10. Period of TFT Multivibrator Circuit vs. Elapsed Time Under Continuous Operation



Original

After 20,000 hr operation

Fig. 11. Device I/V Characteristics Before and After 20,000 hr. Test

good potential. Over 100 hr of noncontinuous operation on a 6 in., 20 lines/inc. display has been obtained without a significant matrix defect occurring.

7. Conclusions

1. The extension of the previously proven 6" x 6" 20 lpi technology to 30 lpi is now well established and good quality displays were made in this period.
2. The second level electroding process to increase the percent lit area is now reliable.
3. The methods have also been reconfigured under a contract modification and displays compatible with an Army field terminal (the ARTADS-DMD) fabricated.

8. Anticipated Results Next Quarter

1. Several good quality DMD formatted displays fabricated using X-Y method.
2. Displays rigorously tested for performance, life, and environmental properties.
3. First attempt at integration of DMD display with the compatible thin film scanning circuit recently developed under Westinghouse support.

9. Contributing Personnel

Dr. T. P. Brody

Dr. Z. P. Szepesi

D. W. Yanda*

Dr. D. H. Davies*

Dr. E. W. Greeneich

D. Leksell*

Dr. F. C. Luo*

W. A. Hester*

*Those persons indicated worked essentially full time on the Contract (~ 400 hrs).

9. Publications, Reports, Conferences and Lectures

The following paper was presented

"Real Time Video Performance on TFT-EL Displays" by T. P. Brody,
F. C. Luo, Z. P. Szepesi, D. H. Davies, P. Kennedy, AGED/IEEE and
Soc. of Info. Display, Joint Biennial Conference, NY, 1976.

Although the work reported was principally supported by
Westinghouse this program reported here was also a contributory
factor and was so acknowledged.

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